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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/417,016	10/12/1999	SHIGEHIRO MASUJI	P63935US0	6885

7590 12/14/2005

JACOBSON PRICE HOLMAN & STERN
PROFESSIONAL LIMITED LIABILITY COMPANY
400 SEVENTH STREET N W
WASHINGTON, DC 20004

EXAMINER	
LESPERANCE, JEAN E	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/417,016	MASUJI ET AL.	
	Examiner	Art Unit	
	Jean E Lesperance	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-13,15,17-20,28,29 and 31-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-13, 15, 17-20, 28, 29 and 31-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on September 21, 2005 is entered and claims 11-13, 15, 17-20, 28, 29 and 31-33 are pending.

2. The rejections under 35 USC 112, first and second paragraphs of the previous Office Action are withdrawn.

Response to Arguments

3. Applicant's arguments with respect to claims 11-13, 15, 17-20, 28, 29 and 31-33 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 11 and 28 are rejected under 35 U.S.C. 102(e) as being unpatentable over US Patent # 6,091,398 ("Shigeta").

Regarding claim 11, Shigeta teaches an apparatus for processing a video signal (the video signal to pixel data corresponding to individual pixels of the self light-emitting display unit (column 2, lines 37 and 38) comprising:

a detector to detect color gradation levels of an input video signal (a viewer would visually sense the luminescence corresponding to the time for sustaining the light emission state (column 4, lines 46-46));

a generator to generate a plurality of dither coefficient signals, each coefficient signal carrying dither coefficients arranged in a matrix (a dither generator 310 repeatedly generates a dither coefficient a, dither coefficient "c", dither coefficient "b" and dither coefficient "d" in circulation for each second clock signal CK2, and supplies those dither coefficients to the adder 320 (column 5, lines 14-18)), weighting being applied to each dither coefficient for components of the input video signal (the column electrode driver 6 separates one frame of pixel drive data read from the frame memory 4 for each of bits with the same weight, generates a pixel data pulse having a voltage value corresponding to a logic value "1" or "0" of that bit, and applies the pulse to column electrodes 30.sub.1 to 30.sub.m of the PDP 10 (column 4, lines 27-32), the components having gradation levels equal to or lower than a predetermined level (it is inherent in the prior art looking at figure 14 that the gradation levels being equal or lower than a predetermined level (Fig.14A, B, C, D), the gradation levels being divided into low to high gradation groups in the order of level of the gradation, in which the weighting to be applied is constant in each gradation group whereas larger for lower gradation groups (a plurality of subframes having light emission periods corresponding to

individual bit positions of pixel drive data, further divides a subframe corresponding to a bit position with a heavy weight into a plurality of subframes, and causes pixels of said self light-emitting display unit to emit light only in those subframes associated with said pixel drive data (column 11, lines 27-33)); and

an adder to add one of the coefficient signals to the components of the input video signal, thus outputting a video signal (The adder 320 adds the aforementioned dither coefficients to the pixel data D sequentially supplied from the A/D converter 1 one by one as shown in FIGS. 4E, 5E, 6E and 7E, and sends the resultant dither-added pixel data to an upper-bit extractor 330 (column 5, lines 36-40)).

wherein each coefficient signal carrying positive and negative coefficients arranged in an (n x m) matrix where "n" and "m" being positive integers larger than zero, the sum total of the coefficients being zero.

Regarding claim 28, Shigeta teaches an apparatus for processing a video signal (the video signal to pixel data corresponding to individual pixels of the self light-emitting display unit (column 2, lines 37 and 38) comprising:

detecting color gradation levels of an input video signal (a viewer would visually sense the luminescence corresponding to the time for sustaining the light emission state (column 4, lines 46-46));

a generating a plurality of dither coefficient signals, each coefficient signal carrying dither coefficients arranged in a matrix (a dither generator 310 repeatedly generates a dither coefficient a, dither coefficient "c", dither coefficient "b" and dither coefficient "d" in circulation for each second clock signal CK2, and supplies

those dither coefficients to the adder 320 (column 5, lines 14-18)), weighting being applied to each dither coefficient for components of the input video signal (the column electrode driver 6 separates one frame of pixel drive data read from the frame memory 4 for each of bits with the same weight, generates a pixel data pulse having a voltage value corresponding to a logic value "1" or "0" of that bit, and applies the pulse to column electrodes 30.sub.1 to 30.sub.m of the PDP 10 (column 4, lines 27-32), the components having gradation levels equal to or lower than a predetermined level (it is inherent in the prior art looking at figure 14 that the gradation levels being equal or lower than a predetermined level (Fig.14A, B, C, D), the gradation levels being divided into low to high gradation groups in the order of level of the gradation, in which the weighting to be applied is constant in each gradation group whereas larger for lower gradation groups (a plurality of subframes having light emission periods corresponding to individual bit positions of pixel drive data, further divides a subframe corresponding to a bit position with a heavy weight into a plurality of subframes, and causes pixels of said self light-emitting display unit to emit light only in those subframes associated with said pixel drive data (column 11, lines 27-33)); and

an adding to the coefficient signals to the components of the input video signal, thus outputting a video signal (The adder 320 adds the aforementioned dither coefficients to the pixel data D sequentially supplied from the A/D converter 1 one by one as shown in FIGS. 4E, 5E, 6E and 7E, and sends the resultant dither-added pixel data to an upper-bit extractor 330 (column 5, lines 36-40)).

Allowable Subject Matter

5. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 13, 15, 17-20, 29 and 31-33 are allowed.

7. The following is an examiner's statement of reasons for allowance: the claimed invention is directed to an apparatus for processing a video signal.

Independent claims 13 and 29 identify a uniquely distinct feature "an adjuster to adjust the dither coefficients of the second dither coefficients pattern signal so that the sum total of the dither coefficients of the second dither coefficients pattern signal is zero, thus producing a third dither coefficients pattern signal carrying the adjusted dither coefficients; and an adder to add the third dither coefficient-adjusted pattern signal to the input video signal, thus outputting a video signal carrying the dot data to be supplied to the display panel".

The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure. Shigeta (6,091,398).

The closest art, Shigeta as discussed above, either singularly or in combination, fails to anticipate or render obvious the above limitations obvious.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (571)

272-7692. The examiner can normally be reached on from Monday to Friday between 10:OOAM and 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Patrick Edouard, can be reached on (571) 272-7603.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(571) 273-8300 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office Whose telephone number is (703) 306-0377.

Jean Lesperance

Art Unit 2674

Date 12/5/2005

PATRICK N. EDOUARD
SUPERVISORY PATENT EXAMINER